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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,184	06/26/2000	Hirohisa Suzuki	81784.0211	3365

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EXAMINER

RAMOS FELICIANO, ELISEO

ART UNIT PAPER NUMBER

2687

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/603,184

Applicant(s)

SUZUKI ET AL.

Examiner

Eliseo Ramos-Feliciano

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 14, 2005 has been entered.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 8-9** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding **claim 8**, it is not clear: how is it possible that a delay time of said first delay circuit corresponds to a sum of an interpolation processing time of said interpolation circuit and a delay time of said second delay circuit, without considering the delay time introduced by the claimed LPF?

**Claim 9** depends on *claim 8*; therefore, contains same problem.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

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such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 1-2 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisch (U.S. Patent Number 5,337,089) in view of Auld et al. (U.S. Patent Number 6,411,333).

Regarding **claim 1**, Fisch discloses a noise cancel circuit (circuit to avoid aliasing noise: anti-aliasing filtering – column 5, lines 19-20; column 1, lines 43-44) for removing noise components (aliasing noise) in a detected radio signal (radio transmission signal – column 4, lines 38-39), including:

an interpolation circuit (vertical filter 68, Figure 8, provides interpolation – column 10, lines 13-14) for performing interpolation processing on said detected radio signal (67 – Figure 8), and

an LPF (vertical filter 68, Figure 8, includes a low-pass filter – column 10, line 9) for eliminating low frequency components of the detected radio signal, wherein

during generation of a pulse noise, a noise portion of said detected radio signal (first path including delay circuit 69 – Figure 8) is interpolated by an output signal (second path including vertical filter 68 – Figure 8) from said interpolation circuit (column 9, line 64 to column 10, lines 15).

However, Fisch fails to specifically disclose the specific configuration of the LPF with respect to the interpolation circuit as defined by applicant: an output of the LPF being provided to the interpolation circuit and the interpolation circuit performing an interpolation process on the output from the LPF. Nevertheless, such configuration is notoriously well known as shown by Auld et al.

In the same filed of endeavor, Auld et al. discloses that a vertical filter 440 (such as Fisch's vertical filter 68) includes a low-pass filter 920 (LPF) and an interpolator 970 – Figure 9B; see column 10, lines 46-49. An output of the LPF being provided to the interpolation circuit and the interpolation circuit performing an interpolation process on the output from the LPF. The advantage of Auld et al.'s circuit configuration is to prevent aliasing noise (same problem Fisch solves) (column 10, lines 61-62); for example, in a detected radio signal (column 4, line 43).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Fisch and Auld et al. to obtain an output of the LPF being provided to the interpolation circuit and the interpolation circuit performing an interpolation process on the output from the LPF, because they both solve the same problem as explained above and for the advantage of better preventing aliasing noise in a detected radio signal as suggested by Auld et al.

Regarding **claim 2**, Fisch and Auld et al. disclose everything claimed as applied above (see *claim 1*). In addition, Auld et al. teaches that the interpolation circuit (interpolator 970 – Figure 9B) executes spline interpolation (uses a cubic spline algorithm – column 11, lines 46-48).

Regarding **claim 10**, Fisch and Auld et al. disclose everything claimed as applied above (see *claim 1*). In addition, Auld et al. teaches that the radio signal is an audio signal (stereo audio – column 4, line 11). Furthermore, Fisch's signal can also be or include audio because it can be an HDTV signal (column 1, line 35).

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5. **Claims 3-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisch and Auld et al. as applied to *claim 1* above, and further in view of the Admitted Prior Art (Figure 3, and page 1, line 17 to page 2, line 9 of the present disclosure).

Regarding **claim 3**, Fisch and Auld et al. disclose everything claimed as applied above (see *claim 1*). In addition, Fisch discloses a selection circuit (switch  $S_5$  – Figure 8) operated by a control signal ( $n \bmod 2$ ) that enables a portion of the detected radio signal to be interpolated by the interpolation circuit according to an output signal (control signal:  $n \bmod 2$ ).

However, the combination fails to specifically disclose a noise detection circuit for detecting the noise portion of said detected radio signal and that the control output signal comes from the noise detection circuit as defined by applicant.

In the same field of endeavor, the prior art admitted by applicant, depicted in Figure 3, and disclosed on page 1, line 17 to page 2, line 9 (herein simply “the Admitted Prior Art”) teaches a noise cancel circuit for removing noise components in a detected radio signal (31). The circuit includes a noise detection circuit (34) for detecting the noise portion of the detected radio signal, so that the noise portion of the detected radio signal is eliminated according to an output signal from the noise detection circuit. That is, when noise is in fact detected, an output signal from the noise detection circuit enables a switch (36) to cancel the noise portion of the detected radio signal. The advantage of the Admitted Prior Art is that the noise detection circuit (34) enables noise cancellation when needed, which is, when noise is in fact detected; thereby improving the overall performance of the circuit.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Fisch and Auld et al. with the Admitted Prior Art to add a

noise detection circuit for detecting the noise portion of the detected radio signal, so that the control output signal comes from the noise detection circuit as defined by applicant, because such combination enables noise cancellation when needed, that is, when noise is in fact detected; thereby improving the overall performance of the circuit.

Regarding **claim 4**, Fisch, Auld et al. and the Admitted Prior Art disclose everything claimed as applied above (see *claim 3*). In addition, Fisch discloses that the noise cancel circuit further includes

a first delay circuit (delay 69 – Figure 8) for delaying said detected radio signal;

a selection circuit (switch  $S_5$  – Figure 8) for selecting either the output signal from said interpolation circuit (path including 68) or the delayed detected radio signal (path including 69) from said first delay circuit, wherein

said selection circuit is controlled according to the output signal from said noise detection circuit (feature explained above in claim 3; explanation that is incorporated herein by reference).

Regarding **claim 5**, Fisch, Auld et al. and the Admitted Prior Art disclose everything claimed as applied above (see *claim 4*). In addition, the interpolation circuit performs interpolation processing and outputs an interpolation signal regardless of presence or absence of noise components, because the interpolator is “always ON” (there is no switch that turns OFF the interpolator in neither of the cited references). See e.g. Figure 8 of Fisch, and Figure 9B of Auld et al.

Regarding **claim 6**, Fisch, Auld et al. and the Admitted Prior Art disclose everything claimed as applied above (see *claim 5*). In addition, Fisch discloses two paths: one containing first delay circuit 69, another containing vertical filter 69 (interpolator and LPF and explained

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above; explanation that is incorporated herein by reference), and elements 70 and 72. It should be noticed that elements 70 and 72 introduce a second delay as claimed; therefore, a second delay circuit (elements 70 and 72) for delaying said interpolation signal from said interpolation circuit.

Regarding **claim 7**, Fisch, Auld et al. and the Admitted Prior Art disclose everything claimed as applied above (see *claim 6*). However, the combination fail to disclose that said second delay circuit is disposed in a processing stage prior to said interpolation circuit as defined by applicant.

The examiner contends that relocation of the delay circuit would be an engineering design choice, as long as the timing match disclosed at column 10, lines 3-5 of Fisch is maintained.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination so that the second delay circuit is disposed in a processing stage prior to said interpolation circuit because of particular design choice.

Regarding **claim 8**, Fisch, Auld et al. and the Admitted Prior Art disclose everything claimed as applied above (see *claim 6*). In addition, Fisch discloses that "the first transmission path simply includes a delay unit 69 which equalizes the delay in the second transmission path" – column 10, lines 3-5. Therefore, a delay time of said first delay circuit (69) corresponds to a sum of an interpolation processing time of said interpolation circuit (68) and a delay time of said second delay circuit (70 and 72).

Regarding **claim 9**, Fisch, Auld et al. and the Admitted Prior Art disclose everything claimed as applied above (see *claim 8*). In addition, Fisch discloses that "the first transmission

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path simply includes a delay unit 69 which equalizes the delay in the second transmission path" – column 10, lines 3-5. Therefore, the delay time of said second delay circuit (70 and 72) corresponds to a difference obtained by subtracting the interpolation processing time of said interpolation circuit (68) from a time delay between generation and detection of said pulse noise.

***Response to Arguments***

6. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

7. Any inquiry concerning this communication from the examiner should be directed to Eliseo Ramos-Feliciano whose telephone number is 571-272-7925. The examiner can normally be reached from 8:00 a.m. to 5:30 p.m. on 5-4/9 1st Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester G. Kincaid, can be reached on (571) 272-7922. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
**ELISEO RAMOS-FELICIANO**  
**PATENT EXAMINER**

ERF/erf  
May 5, 2005